What is claimed is:

Sub a1

1. A liquid crystal display device having a liquid crystal display panel and liquid crystal drive circuitry, wherein the liquid crystal drive circuitry comprises:

an image input terminal with an image signal being input thereto;

a clock input terminal with an external clock signal being input thereto;

a clock compensation circuit for generating an internal clock based on the external clock signal, the internal clock signal swinging from a first voltage to a second voltage lower than the first voltage;

a data storage circuit for storing therein an image signal at a timing of a voltage change of the internal clock signal;

a data bus causing the image signal to be output from the data storage circuit; and

a voltage select circuit for selecting from the image signal of the data bus a voltage used to drive the liquid crystal display panel and then outputting the voltage selected.

Sub B1

2. The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has a phase locked loop circuit.

3. The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has a delay locked

loop circuit.

4. The liquid crystal display device as claimed in Claim 1, wherein the data bus comprises two systems of signal lines.

Sub a2 5. A liquid crystal display device having a liquid crystal display element and liquid crystal drive circuitry, wherein the liquid crystal drive circuitry comprises:

a data input terminal with an image signal being input thereto;

a clock compensation circuit for inputting an external clock and outputting an internal clock, the internal clock having a first period for permitting output of a first voltage and a second period for output of a second voltage;

a data latch circuit for taking thereinto an image signal at a timing of a change of the internal clock;

a data bus for output of the image signal from the data latch circuit;

a voltage output circuit for outputting a voltage from the image signal on the data bus to the liquid crystal display element;

a data output circuit for outputting the image signal on the data bus to a next stage of liquid crystal drive circuit; and

the clock formation circuit being operable to correct the internal clock based on the external clock.

Sub B1 6. The liquid crystal display device as claimed in Claim

5, wherein the clock formation circuit has a phase locked loop circuit.

7. The liquid crystal display device as claimed in Claim 5, wherein the clock formation circuit has a delay locked loop circuit.

8. The liquid crystal display device as claimed in Claim 5, wherein the data bus comprises tow systems of signal lines.

add a3